THAT WHICH IS CLAIMED IS:

1. A serial peripheral interface comprising:

a RAM memory coupled to at least an external data bus (DATA IN, DATA OUT) for transferring data to be transmitted or received from a peripheral and an external address bus (ADDR) for receiving addresses at which to store data to be transmitted or received, having a memory section for storing data to be transmitted (TRANSMIT RAM), a memory section for storing received data (RECEIVE RAM) and a memory section for storing configuration commands of the interface (COMMAND RAM; MODE RAM);

circuit means for generating pointers (POINTER, CURRENT POINTER, END POINTER, COMP) to the single bits of an addressed memory location of said memory sections;

circuit means for serial transfer of data (TRANSMIT SHIFT REGISTER, RECEIVE SHIFT REGISTER, PIN CONTROL LOGIC) from or to at least a peripheral connected to the interface, coupled to said memory and for executing a certain configuration command; and

a control register (CTRL) coupled to said memory and to said circuit means for serial transfer, controlling the data transfer to be transmitted or received;

characterized in that

said memory sections for storing data (TRANSMIT RAM, RECEIVE RAM) are divided in distinct memory spaces and each memory space is destined to store data pertaining to a respective peripheral connected to the interface;

said memory section for storing configuration commands (MODE RAM) contains all the configuration commands of the interface for communicating with all the peripherals connected to it;

said interface further comprises a circuit for generating addresses (POINTER RAM) to said memory section containing all the configuration commands (MODE RAM), input with addresses provided on said external address bus (ADDR) and generating, in function of the address on the external address bus, a corresponding address in which the relative configuration command to be executed is stored.

2. The interface of claim 1, wherein said memory section for storing configuration commands (MODE RAM) of the interface is a second RAM memory distinct from said first memory.

3. A serial communication device, comprising:

a serial peripheral interface, that may be coupled to at least a peripheral with which to communicate, having at least a memory for storing data conveyed through it;

at least an internal data bus (DATA IN, DATA OUT) for transferring data from or to the interface and an address bus (ADDR) for said memory in which said data in transit must be stored; and

a microprocessor unit coupled to said data bus (DATA IN, DATA OUT) and to said address bus (ADDR);

characterized in that

said interface is a serial peripheral interface of one of claims 1 and 2.

4. Method of managing a serial peripheral interface as defined in one of claims 1 and 2, comprising the following operations:

initializing the interface by loading in said memory section for storing commands (MODE RAM) all the configuration commands of the interface for

communicating with all the peripherals connected to it;

associating to each connected peripheral a respective memory space in both said memory sections for storing data (TRANSMIT RAM, RECEIVE RAM);

for each address on said address bus (ADDR), generating a corresponding address of the memory section containing the configuration commands (MODE RAM);

for transmitting a datum to a certain peripheral, sending on said address bus (ADDR) an address (X) of the memory section for storing data to be transmitted (TRANSMIT RAM) associated to said peripheral, and configuring the interface according to the command stored at said generated corresponding address of the memory section containing the configuration commands (MODE RAM); and

for receiving a datum from a certain peripheral, sending on said address bus (ADDR) an address (Y) of the memory section for storing received data (RECEIVE RAM) associated to said peripheral, and configuring the interface according to the command stored at said generated corresponding address of the memory section containing the configuration commands (MODE RAM).